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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Filed: April 2, 2001
Inventor(s):
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Title: Selective Zero Extension Based on Operand Size

Examiner: Gerstl, Shane F.
Group/Art Unit: 2183
Atty. Dkt. No: 5500-64000

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APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
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Sir/Madam:

Further to the Notice of Appeal filed September 13, 2004, Appellants present this Appeal Brief. Appellants respectfully request that this appeal be considered by the Board of Patent Appeals and Interferences.

I. REAL PARTY IN INTEREST

The present application is owned by Advanced Micro Devices, Inc., a corporation organized and existing under and by virtue of the laws of the State of Delaware, and having its principal place of business at One AMD Place, Sunnyvale, CA 94088, as evidenced by the assignment recorded at Reel 011766, Frame 0119.

II. RELATED APPEALS AND INTERFERENCES

No other appeals, interferences or judicial proceedings are known which would be related to, directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-2, 8-11, 13-14, 17-18, and 20-37 are pending and rejected. Claims 3-7, 12, 15-16, and 19 were previously cancelled. The rejection of claims 1-2, 8-11, 13-14, 17-18, and 20-37 is being appealed. A copy of claims 1-2, 8-11, 13-14, 17-18, and 20-37 is included in the Claims Appendix attached hereto.

IV. STATUS OF AMENDMENTS

No amendments to the claims have been submitted subsequent to the final rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a processor comprising a register and an execution core coupled to the register (see, e.g., Fig. 1, reference numerals 14 and 22 where the register may be any of the registers in the register file 22). The register is configured to store a first number of bits. The execution core is configured to execute an instruction to produce a result, wherein the instruction has the register as a destination

(see, e.g., specification page 10, line 25 to page 11, line 7 and page 18, lines 16-19). The execution core is configured to zero extend the result for update in the register or to preserve a value of at least a portion of the bits in the register dependent on the operand size corresponding to the instruction (see, e.g., specification, page 17, lines 1-22). Particularly, responsive to an operand size corresponding to the instruction specifying a second number of bits less than the first number of bits that the register is configured to store, the execution core is configured to zero extent the result. Responsive to the operand size specifying a third number of bits less than the first number of bits and different from the second number, the execution core is configured to preserve a value of at least a portion of the bits in the register that are not updated by the result. Various embodiments of the zero extension and preservation are shown in Figs. 5-9 and described in the specification at page 18, line 9 to page 24, line 4. Independent claim 13 is directed to a similar method and independent claim 32 is directed to a computer system comprising the processor and an input/output device configured to communicate between the computer system and another computer system. (See, e.g., Figs. 10 and 11, reference numerals 200 and 300 and specification page 24, line 6 to page 29, line 11).

Independent claim 20 is directed to an apparatus comprising a storage location corresponding to a register and an execution circuit coupled to the storage location (See, e.g., Fig. 1, reference numerals 14 and 22, and/or Figs. 14, 15, and 16, reference numerals 1042 and 1052). The register is defined to store a first number of bits. The execution circuit is configured to execute an instruction to produce a result, wherein the instruction has the register as a destination (see, e.g., specification page 10, line 25 to page 11, line 7; page 18, lines 16-19; and page 29, line 13 to page 30, line 11). The execution circuit is configured to zero extend the result for update in the storage location responsive to an operand size corresponding to the instruction specifying a second number of bits less than the first number of bits, or to preserve a value of at least a portion of the bits in the storage location that are not updated by the result responsive to the operand size specifying a third number of bits less than the first number of bits and different from the second number (see, e.g., specification, page 17, lines 1-22). Various embodiments of

the zero extension and preservation are shown in Figs. 5-9 and described in the specification at page 18, line 9 to page 24, line 4.

Independent claim 26 is directed to an apparatus comprising a storage location corresponding to a register and an execution circuit coupled to the storage location (See, e.g., Fig. 1, reference numerals 14 and 22, and/or Figs. 14, 15, and 16, reference numerals 1042 and 1052). The register is defined to store a first number of bits. The execution circuit is configured to extend the result to the first number of bits for update in the storage location responsive to an operand size corresponding to the instruction specifying a second number of bits less than the first number of bits, or to preserve a value of at least a portion of the bits in the storage location that are not updated by the result responsive to the operand size specifying a third number of bits less than the first number of bits and different from the second number (see, e.g., specification, page 17, lines 1-22). Independent claim 35 is directed to a computer system comprising a processor embodiment similar to the apparatus of claim 26 and an input/output device configured to communicate between the computer system and another computer system. (See, e.g., Figs. 10 and 11, reference numerals 200 and 300 and specification page 24, line 6 to page 29, line 11).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-2, 8-11, 13-14, 17-18, 20-32, and 35 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Killian et al., U.S. Patent No. 5,420,992 ("Killian").

2. Claims 33 and 36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Killian in view of The Authoritative Dictionary of IEEE Standards Terms, 2000 ("IEEE").

3. Claims 34 and 37 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Killian in view of "Computer Architecture: A Quantitative Approach", Hennessy and Patterson, 1990 ("Hennessy").

VII. <u>ARGUMENT</u>

<u>First Ground of Rejection</u>:

Claims 1-2, 8-11, 13-14, 17-18, 20-32, and 35 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Killian. Appellants traverse this rejection for the following reasons.

<u>Claims 1, 2, 13, 14, 20, 21, 26, 27, 32, and 35</u>:

Appellants respectfully submit that each of claims 1, 2, 13, 14, 20, 21, 26, 27, 32, and 35 recite combinations of features not taught or suggested in Killian. For example, each of claims 1 and 32 recite a combination of features including: "said execution core is configured to <u>execute an instruction to produce a result</u>, said instruction having said register as a destination, and wherein said execution core is configured to <u>zero extend said result for update in said register responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits</u>, and wherein said execution core is configured to <u>preserve a value of at least a portion of said bits in said register that are not updated by said result [of said instruction] responsive to said operand size [corresponding to said instruction] specifying a third number of bits</u> less than said first number of bits and different from said second number". Appellants have added [of said instruction] and [corresponding to said instruction] above merely to further highlight the patentability of claims 1 and 32 over Killian. The antecedent basis of "said operand size" and "said result" in the "preserve a value" phrase makes it clear that the same instruction, result, and operand size are referred to throughout the claim.

The Final Office Action mailed June 17, 2004 in the present application (the "Final Office Action" herein) alleges that Killian anticipates the above highlighted features. However, the Final Office Action cites <u>two separate and distinct instructions</u> from Killian to allegedly teach the above features. Specifically, the Office Action uses the LBU (load byte unsigned) instruction to allegedly teach "said execution core is configured to zero extend said result for update in said register responsive to an operand

size corresponding to said instruction specifying a second number of bits" and the ORI (logical OR immediate) instruction to allegedly teach "said execution core is configured to preserve a value of at least a portion of said bits in said register that are not updated by said result responsive to said operand size specifying a third number of bits". See Final Office Action, page 3, line 17 to page 4, line 10.

These two separate instructions cannot anticipate "said execution core is configured to execute an instruction to produce a result ... said execution core is configured to zero extend *said result* for update in said register responsive to *an operand size corresponding to said instruction specifying* a second number of bits less than said first number of bits, and wherein said execution core is configured to preserve a value of at least a portion of said bits in said register that are *not updated by said result [of said instruction]* responsive to *said operand size [corresponding to said instruction] specifying* a third number of bits less than said first number of bits and different from said second number". Appellants respectfully submit that Killian does not teach or suggest an execution core having the above features.

The Advisory Action mailed August 13, 2004 in the present application (the "Advisory Action" herein) states the claim language does not limit the zero extending and the preserving to the same instruction, relying on the operand size possibly corresponding to other instructions. However, this analysis ignores the clear antecedent basis of said result, also referred to in the "preserve" phrase above, which refers back to the result of the instruction being described in the claim. Appellants respectfully submit that, when the combination of features recited in each of claims 1 and 32 is read as a whole, it is very clear that the same instruction is being referred to in the extending and preserving portions of the claim. Thus, to properly anticipate the combination of features recited in claim 1, Killian must teach an instruction for which an execution core is "configured to zero extend *said result* for update in said register responsive to *an operand size corresponding to said instruction specifying* a second number of bits less than said first number of bits" and for which the execution core is "configured to preserve a value of at least a portion of said bits in said register that are *not updated by said result [of said*

instruction] responsive to *said operand size [corresponding to said instruction] specifying* a third number of bits less than said first number of bits and different from said second number". Appellants submit that Killian includes no such teaching, and thus Killian fails to anticipate the above highlighted combination of features.

Claim 13 recites a combination of features including: "executing an instruction to produce a result ... zero extending said result for update in said register responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits; and preserving a value of at least a portion of said bits in said register that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number." The same teachings of Killian highlighted above with regard to claim 1 are also alleged to teach the above highlighted combination of features of claim 13. Appellants respectfully submit that the teachings of Killian do not anticipate the above highlighted features of claim 13 either.

Claim 20 recites a combination of features including: "said execution circuit is configured to execute an instruction to produce a result ...said execution core is configured to zero extend said result for update in said storage location responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution circuit is configured to preserve a value of at least a portion of said bits in said storage location that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number". The same teachings of Killian highlighted above with regard to claim 1 are also alleged to teach the above highlighted combination of features of claim 20. Appellants respectfully submit that the teachings of Killian do not anticipate the above highlighted features of claim 20 either.

Claim 26 recites a combination of features including "said execution circuit is configured to execute an instruction to produce a result, said instruction having said register as a destination, and wherein said execution core is configured to extend said

result to said first number of bits for update in said storage location responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution circuit is configured to preserve a value of at least a portion of said bits in said storage location that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number". The same teachings of Killian highlighted above with regard to claim 1 are also alleged to teach the above highlighted combination of features of claim 26. Appellants respectfully submit that the teachings of Killian do not anticipate the above highlighted features of claim 26 either.

Claim 35 recites a combination of features including: "said execution core is configured to execute an instruction to produce a result, said instruction having said register as a destination, and wherein said execution core is configured to extend said result to said first number of bits for update in said register responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution core is configured to preserve a value of at least a portion of said bits in said register that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number". The same teachings of Killian highlighted above with regard to claim 35 are also alleged to teach the above highlighted combination of features of claim 35. Appellants respectfully submit that the teachings of Killian do not anticipate the above highlighted features of claim 35 either.

For at least the above stated reasons, Appellants respectfully submit that the rejection of claims 1, 13, 20, and 32 is in error and respectfully request reversal of the rejection. Claims 2, 14, 21, and 27 depend from claims 1, 13, 20, and 26, respectively, and thus are patentable over Killian for at least the reasons given above for claims 1, 13, 20, and 26.

Claims 8, 22, and 28:

Claims 8, 22, and 28 depend from claims 1, 20, and 26, respectively, and thus are patentable over Killian for at least the reasons given above for claims 1, 20, and 26. Additionally, Appellants respectfully submit that each of claims 8, 22, and 28 recite combinations of features not taught or suggested in Killian. For example, claim 8 recites a combination of features including: "said execution core is coupled to receive an operating mode of said processor, and wherein said execution core is configured to zero extend said result [for update in said register, from claim 1] further responsive to said operating mode".

The Final Office Action alleges that the above features are taught in Killian at col. 3, lines 38-55 and that col. 3, line 56-col. 4, line 10 illustrates how these modes affect zero extending and sign extending configurations (see Final Office Action, page 4, item 9). However, Killian col. 3, lines 38-55 is discussing the address size in the processor dependent on user, supervisor, or kernel modes. In col. 3, line 56-col. 4, line 10, Killian describes how address generation is affected by the modes, and describes various sign extension and zero extension options in the address generation path of the processor. These addresses are not the result of an instruction, to be updated in a register, as recited in claim 8 (and claim 1 upon which claim 8 depends).

For example, Killian teaches "A straightforward approach for the m-bit mode is to provide sign-extension hardware *in the virtual address path* to guarantee a sign-extended output in the event of m-bit two's complement overflow. However, where timing constraints militate against such sign-extension, it suffices to force the (N-m) most significant bits to zero. Accordingly, in one embodiment, zeroing circuitry is provided in the *path to the address translation unit*. This circuitry is invoked for m-bit user mode while the most significant (N-m) bits are passed unchanged in m-bit kernel mode and N-bit mode" (Killian, col. 3, line 67-col. 4, line 10). Nothing in Killian's teachings regarding address size and sign or zero extension of addresses anticipates "said execution core is coupled to receive an operating mode of said processor, and wherein said

execution core is configured to zero extend said result [for update in said register, from claim 1] further responsive to said operating mode" as recited in claim 8.

Claim 22 recites a combination of features including: "said execution circuit is coupled to receive an operating mode, and wherein said execution circuit is configured to zero extend said result further responsive to said operating mode". The same teachings of Killian highlighted above with regard to claim 8 are also alleged to teach the above highlighted combination of features of claim 22. Appellants respectfully submit that the teachings of Killian do not anticipate the above highlighted features of claim 22 either.

Claim 28 recites a combination of features including: "said execution circuit is coupled to receive an operating mode, and wherein said execution circuit is configured to selectively extend said result further responsive to said operating mode". The same teachings of Killian highlighted above with regard to claim 8 are also alleged to teach the above highlighted combination of features of claim 28. Appellants respectfully submit that the teachings of Killian do not anticipate the above highlighted features of claim 28 either.

For at least the above stated reasons, Appellants respectfully submit that the rejection of claims 8, 22, and 28 is in error and respectfully request reversal of the rejection.

Claims 9, 23, and 29:

Claims 9, 23, and 29 depend from claims 8, 22, and 28, respectively, and thus are patentable over Killian for at least the reasons given above for claims 8, 22, and 28. Additionally, Appellants respectfully submit that each of claims 9, 23, and 29 recite combinations of features not taught or suggested in Killian. For example, each of claims 9, 23, and 29 recite a combination of features including: "said operating mode includes a default operand size, and wherein said operand size corresponding to said instruction is said default operand size unless overridden by an encoding of said instruction".

The Final Office Action alleges that the default operand size is shown in col. 3, lines 58-64 of Killian, where the mode specifies the operand size via the instruction size of the program (see Final Office Action, page 5, item 10). Appellants respectfully disagree. Killian teaches " In a particular implementation, the previous architecture allowed valid user <u>addresses</u> (MSB=0) to result from two's complement overflow. In order to handle this special case in the extended architecture it is necessary to provide <u>an address mode</u> in the machine's status register to specify whether the machine is running an m-bit program (i.e., one written for the previous architecture) or an N-bit program (i.e., one written for the extended architecture). In m-bit user mode, it is necessary to <u>sign-extend the address</u> when two's complement overflow occurs." (Killian, col. 3, lines 58-64). Thus, these teachings are with regard to the address size of Killian's processor, and do not anticipate "said operating mode includes a default operand size" as recited in claims 9, 23, and 29.

Furthermore, the Final Office Action alleges that in order to recognize the sizes, it is inherent that there is an encoding to specify the size. Appellants respectfully submit that Killian teaches recognizing the address mode using the machine's status register: "In order to handle this special case in the extended architecture it is necessary to provide <u>an address mode in the machine's status register</u> to specify whether the machine is running an m-bit program (i.e., one written for the previous architecture) or an N-bit program (i.e., one written for the extended architecture)." (Killian, col. 3, lines 58-64). Thus, the address mode is not part of an instruction encoding. Still further, these teachings describe address sizes, not operand sizes. Accordingly, Killian also does not anticipate "said <u>operand size corresponding to said instruction is said default operand size unless overridden by an encoding of said instruction</u>".

For at least the above stated reasons, Appellants respectfully submit that the rejection of claims 9, 23, and 29 is in error and respectfully request reversal of the rejection.

Claims 10, 24, and 30:

Claims 10, 24, and 30 depend from claims 9, 23, and 29, respectively, and thus are patentable over Killian for at least the reasons given above for claims 9, 23, and 29. Additionally, Appellants respectfully submit that each of claims 10, 24, and 30 recite combinations of features not taught or suggested in Killian. For example, claim 10 recites a combination of features including: "said execution core is configured to zero extend said result if said operand size is said default operand size". Claim 24 recites a combination of features including "said execution circuit is configured to zero extend said result if said operand size is said default operand size". Claim 30 recites a combination of features including: "said execution circuit is configured to extend said result to said first number of bits if said operand size is said default operand size".

With regard to claims 10, 24, and 30, the Final Office Action again refers to Killian's teachings regarding address sizes in col. 3, lines 58-64 and the corresponding discussion of sign extension and zero extension of addresses in the address generation path at col. 3, line 67-col. 4, line 10. As highlighted above, these teachings regarding address size do not anticipate the operand size. Thus, Killian also does not anticipate "said execution core is configured to zero extend said result if said operand size is said default operand size" as recited in claim 10 nor "said execution circuit is configured to zero extend said result if said operand size is said default operand size" as recited in claim 24 nor "said execution circuit is configured to extend said result to said first number of bits if said operand size is said default operand size" as recited in claim 30.

For at least the above stated reasons, Appellants respectfully submit that the rejection of claims 10, 24, and 30 is in error and respectfully request reversal of the rejection.

Claims 11, 25, and 31:

Claims 11, 25, and 31 depend from claims 9, 23, and 29, respectively, and thus are patentable over Killian for at least the reasons given above for claims 9, 23, and 29. Additionally, Appellants respectfully submit that each of claims 11, 25, and 31 recite

combinations of features not taught or suggested in Killian. For example, each of claims 11, 25, and 31 recite a combination of features including: "said default operand size is overridden by said encoding if said instruction includes one or more operand size override prefixes."

The Final Office Action alleges that Killian teaches the above highlighted features, interpreting a prefix as "a set of bits". This interpretation is inconsistent with the any reasonable definition of the term "prefix". Generally, a prefix refers to something attached to the front of something else to modify its meaning. Thus, in this context, an operand size override prefix is included at the front of the instruction. Given a reasonable definition of the term "prefix", Killian does not anticipate claims 11, 25, and 31.

For at least the above stated reasons, Appellants respectfully submit that the rejection of claims 11, 25, and 31 is in error and respectfully request reversal of the rejection.

<u>Claim 17</u>:

Claim 17 depends from claims 13 and thus is patentable over Killian for at least the reasons given above for claim 13. Additionally, Appellants respectfully submit that claim 17 recites a combination of features not taught or suggested in Killian. For example, claim 17 recites a combination of features including: "said zero extending and said preserving are further responsive to an operating mode of a processor performing said executing".

The Final Office Action alleges that the above features are taught in Killian at col. 3, lines 38-55 and that col. 3, line 56-col. 4, line 10 illustrates how these modes affect zero extending and sign extending configurations (see Final Office Action, page 7, item 15). However, Killian col. 3, lines 38-55 is discussing the <u>address size</u> in the processor dependent on user, supervisor, or kernel modes. In col. 3, line 56-col. 4, line 10, Killian describes how <u>address generation</u> is affected by the modes, and describes various sign extension and zero extension options in the <u>address generation path</u> of the processor.

These addresses are not the result of an instruction, to be updated in a register, as recited in claim 17 (and claim 13 upon which claim 17 depends).

For example, Killian teaches "A straightforward approach for the m-bit mode is to provide sign-extension hardware *in the virtual address path* to guarantee a sign-extended output in the event of m-bit two's complement overflow. However, where timing constraints militate against such sign-extension, it suffices to force the (N-m) most significant bits to zero. Accordingly, in one embodiment, zeroing circuitry is provided in the *path to the address translation unit*. This circuitry is invoked for m-bit user mode while the most significant (N-m) bits are passed unchanged in m-bit kernel mode and N-bit mode" (Killian, col. 3, line 67-col. 4, line 10). Nothing in Killian's teachings regarding address size and sign or zero extension of addresses anticipates "said zero extending and said preserving are further responsive to an operating mode of a processor performing said executing" as recited in claim 17.

The Final Office Action further alleges that the intermediate value for the OR function will be affected by these modes in the same manner, and thus the preserving is responsive to the modes as well. **There is no teaching or suggestion in Killian to support this assertion**. As highlighted above, the teachings of Killian cited with regard to claim 17 refer to address size and sign extension/zero extension for addresses in the address generation path. There is no reason to assume that operation of the address generation path has any affect on non-address operations such as the immediate value of the OR. Accordingly, Killian cannot anticipate "said preserving ... responsive to an operating mode of a processor performing said executing" as recited in claim 17.

For at least the above stated reasons, Appellants respectfully submit that the rejection of claim 17 is in error and respectfully request reversal of the rejection.

Claim 18:

Claim 18 depends from claim 17, and thus is patentable over Killian for at least the reasons given above for claim 17. Additionally, Appellants respectfully submit that

claim 17 recites a combination of features not taught or suggested in Killian. For example, claim 18 recites a combination of features including: "said operating mode includes a default operand size, and the method further comprises zero extending said result if said operand size is said default operand size."

With regard to claim 18, the Final Office Action again refers to Killian's teachings regarding address sizes in col. 3, lines 58-64 and the corresponding discussion of sign extension and zero extension of addresses in the address generation path at col. 3, line 67-col. 4, line 10. As highlighted above, these teachings regarding address size do not anticipate the operand size. Thus, Killian also does not anticipate "said operating mode includes a default operand size, and the method further comprises zero extending said result if said operand size is said default operand size" as recited in claim 18

For at least the above stated reasons, Appellants respectfully submit that the rejection of claim 18 is in error and respectfully request reversal of the rejection.

Second Ground of Rejection:

Claims 33 and 36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Killian in view of IEEE. Appellants traverse this rejection for the following reasons.

Claims 33 and 36:

Claims 33 and 36 depend from claims 32 and 35, respectively, and thus are patentable over Killian for at least the reasons given above for claims 32 and 35. The Final Office Action relies on IEEE to allegedly teach a modem. Appellants respectfully submit that IEEE also does not teach or suggest the features of claims 32 and 35. Accordingly, claims 33 and 36 are patentable over Killian and IEEE for at least the reasons given above for claims 32 and 35, respectively. Accordingly, Appellants respectfully submit that the rejection of claims 33 and 36 is in error and respectfully request reversal of the rejection.

Third Ground of Rejection:

Claims 34 and 37 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Killian in view of Hennessy. Appellants traverse this rejection for the following reasons.

Claims 34 and 37:

Claims 34 and 37 depend from claims 32 and 35, respectively, and thus are patentable over Killian for at least the reasons given above for claims 32 and 35. The Final Office Action relies on Hennessy to allegedly teach a modem. Appellants respectfully submit that Hennessy also does not teach or suggest the features of claims 32 and 35. Accordingly, claims 34 and 37 are patentable over Killian and Hennessy for at least the reasons given above for claims 32 and 35, respectively. Accordingly, Appellants respectfully submit that the rejection of claims 34 and 37 is in error and respectfully request reversal of the rejection.

VIII. CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejection of claims 1-2, 8-11, 13-14, 17-18, and 20-37 was erroneous, and reversal of the decision is respectfully requested.

The Commissioner is authorized to charge the appeal brief fee of $340.00 and any other fees that may be due to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-64000/LJM. This Appeal Brief is submitted with a return receipt postcard.

Respectfully submitted,

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Date: October 15, 2004

IX. CLAIMS APPENDIX

The claims on appeal are as follows.

1. A processor comprising:

a register configured to store a first number of bits; and

an execution core coupled to said register, wherein said execution core is configured to execute an instruction to produce a result, said instruction having said register as a destination, and wherein said execution core is configured to zero extend said result for update in said register responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution core is configured to preserve a value of at least a portion of said bits in said register that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number.

2. The processor as recited in claim 1 wherein said result comprises a number of bits specified by said operand size.

8. The processor as recited in claim 1 wherein said execution core is coupled to receive an operating mode of said processor, and wherein said execution core is configured to zero extend said result further responsive to said operating mode.

9. The processor as recited in claim 8 wherein said operating mode includes a default operand size, and wherein said operand size corresponding to said instruction is said default operand size unless overridden by an encoding of said instruction.

10. The processor as recited in claim 9 wherein said execution core is configured to zero

extend said result if said operand size is said default operand size.

11. The processor as recited in claim 9 wherein said default operand size is overridden by said encoding if said instruction includes one or more operand size override prefixes.

13. A method comprising:

executing an instruction to produce a result, said instruction having a register as a destination and said register configured to store a first number of bits;

zero extending said result for update in said register responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits; and

preserving a value of at least a portion of said bits in said register that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number.

14. The method as recited in claim 13 wherein said result comprises a number of bits specified by said operand size.

17. The method as recited in claim 13 wherein said zero extending and said preserving are further responsive to an operating mode of a processor performing said executing.

18. The method as recited in claim 17 wherein said operating mode includes a default operand size, and the method further comprises zero extending said result if said operand size is said default operand size.

20. An apparatus comprising:

a storage location corresponding to a register, said register defined to store a first number of bits; and

an execution circuit coupled to said storage location, wherein said execution circuit is configured to execute an instruction to produce a result, said instruction having said register as a destination, and wherein said execution core is configured to zero extend said result for update in said storage location responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution circuit is configured to preserve a value of at least a portion of said bits in said storage location that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number.

21. The apparatus as recited in claim 20 wherein said result comprises a number of bits specified by said operand size.

22. The apparatus as recited in claim 20 wherein said execution circuit is coupled to receive an operating mode, and wherein said execution circuit is configured to zero extend said result further responsive to said operating mode.

23. The apparatus as recited in claim 22 wherein said operating mode includes a default operand size, and wherein said operand size corresponding to said instruction is said default operand size unless overridden by an encoding of said instruction.

24. The apparatus as recited in claim 23 wherein said execution circuit is configured to zero extend said result if said operand size is said default operand size.

25. The apparatus as recited in claim 23 wherein said default operand size is overridden by said encoding if said instruction includes one or more operand size override prefixes.

26. An apparatus comprising:

a storage location corresponding to a register, said register defined to store a first number of bits; and

an execution circuit coupled to said storage location, wherein said execution circuit is configured to execute an instruction to produce a result, said instruction having said register as a destination, and wherein said execution core is configured to extend said result to said first number of bits for update in said storage location responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution circuit is configured to preserve a value of at least a portion of said bits in said storage location that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number.

27. The apparatus as recited in claim 26 wherein said result comprises a number of bits specified by said operand size.

28. The apparatus as recited in claim 26 wherein said execution circuit is coupled to receive an operating mode, and wherein said execution circuit is configured to selectively extend said result further responsive to said operating mode.

29. The apparatus as recited in claim 28 wherein said operating mode includes a default operand size, and wherein said operand size corresponding to said instruction is said default operand size unless overridden by an encoding of said instruction.

30. The apparatus as recited in claim 29 wherein said execution circuit is configured to extend said result to said first number of bits if said operand size is said default operand

size.

31. The apparatus as recited in claim 29 wherein said default operand size is overridden by said encoding if said instruction includes one or more operand size override prefixes.

32. A computer system comprising:

a processor comprising a register configured to store a first number of bits and an execution core coupled to said register, wherein said execution core is configured to execute an instruction to produce a result, said instruction having said register as a destination, and wherein said execution core is configured to zero extend said result for update in said register responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution core is configured to preserve a value of at least a portion of said bits in said register that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number; and

an input/output (I/O) device configured to communicate between said computer system and another computer system.

33. The computer system as recited in claim 32 wherein the I/O device comprises a modem.

34. The computer system as recited in claim 32 further comprising an audio device.

35. A computer system comprising:

a processor comprising a register configured to store a first number of bits and an execution core coupled to said register, wherein said execution core is

configured to execute an instruction to produce a result, said instruction having said register as a destination, and wherein said execution core is configured to extend said result to said first number of bits for update in said register responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution core is configured to preserve a value of at least a portion of said bits in said register that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number; and

an input/output (I/O) device configured to communicate between said computer system and another computer system.

36. The computer system as recited in claim 35 wherein the I/O device comprises a modem.

37. The computer system as recited in claim 35 further comprising an audio device.

X. EVIDENCE APPENDIX

No evidence submitted under 37 CFR §§ 1.130, 1.131 or 1.132 or otherwise entered by the Examiner is relied upon in this appeal.

XI. RELATED PROCEEDINGS APPENDIX

There are no related proceedings.